## CLAIMS

What is claimed is:

1. An apparatus comprising:

a bus arbiter coupled to first and second processors via first and second master buses, respectively, to generate an arbitration select signal based on result of arbitrating bus access information from the first and second processors; and

a first multiplexer coupled to the first and second master buses and a first slave bus in a plurality of slave buses to provide device access information selected from the bus access information using the arbitration select signal, the device access information being transferred to a first slave device connected to the first slave bus.

2. The apparatus of claim 1 wherein the device access information includes at least one of slave address and write data.

3. The apparatus of claim 2 further comprising:

an address decoder coupled to the bus arbiter and the first multiplexer to decode the slave address, the decoded slave address specifying the first slave device, the address decoder generating device select signal.

4. The apparatus of claim 3 further comprising:

a second multiplexer coupled to the first slave bus to provide bus response information from device response information using the device select signal; and

a de-multiplexer coupled to the second multiplexer and the first and second master buses to transfer the bus response information to one of the first and second processors using the arbitration select signal.

5. The apparatus of claim 4 wherein the device response information includes at least one of device ready status and read data.

6. The apparatus of claim 5 wherein the plurality of slave buses are coupled to a common memory via a common memory interface.

7. The apparatus of claim 5 wherein one of the first and second processors is a direct memory access (DMA) controller.

8. The apparatus of claim 5 wherein one of the first and second processors is a microprocessor.

9. The apparatus of claim 5 wherein the first slave device is one of a memory device and a peripheral device.

10. The apparatus of claim 5 wherein the plurality of slave buses includes at least one of a homogenous set and a heterogeneous set.

11. A method comprising:

generating an arbitration select signal based on result of arbitrating bus access information from first and second processors via first and second master buses, respectively; and

providing device access information selected from the bus access information using the arbitration select signal, the device access information being transferred to a first slave device connected to a first slave bus from a plurality of slave buses.

12. The method of claim 11 wherein providing device access information comprises providing at least one of slave address and write data.

13. The method of claim 12 further comprising:

decoding the slave address, the decoded slave address specifying the first slave device; and

generating device select signal.

14. The method of claim 13 further comprising:

providing bus response information from device response information using the device select signal; and

transferring the bus response information to one of the first and second processors using the arbitration select signal.

15. The method of claim 14 wherein providing the bus response information from device response information comprises providing the bus response information from at least one of device ready status and read data.

16. The method of claim 15 further comprising accessing a common memory via a common memory interface.

17. The method of claim 15 wherein one of the first and second processors is a direct memory access (DMA) controller.

18. The method of claim 15 wherein one of the first and second processors is a microprocessor.

19. The method of claim 15 wherein the first slave device is one of a memory device and a peripheral device.

20. The method of claim 15 wherein the plurality of slave buses includes at least one of a homogenous set and a heterogeneous set.

21. A system comprising:

first and second processors coupled to first and second master buses;

a plurality of slave buses, each of the slave buses coupled to a plurality of slave devices; and

a master bus interface circuit coupled to the first and second master buses and the plurality of slave buses, the master bus interface circuit comprising a plurality of bus controllers, each of the bus controllers comprising:

a bus arbiter coupled to the first and second processors via the first and second master buses, respectively, to generate an

arbitration select signal based on result of arbitrating bus access information from the first and second processors, and

a first multiplexer coupled to the first and second master buses and a first slave bus in the plurality of slave buses to provide device access information selected from the bus access information using the arbitration select signal, the device access information being transferred to a first slave device connected to the first slave bus.

22. The system of claim 21 wherein the device access information includes at least one of slave address and write data.

23. The system of claim 22 wherein each of the bus controllers further comprising:

an address decoder coupled to the bus arbiter and the first multiplexer to decode the slave address, the decoded slave address specifying the first slave device, the address decoder generating device select signal.

24. The system of claim 23 wherein each of the bus controllers further comprising:

a second multiplexer coupled to the first slave bus to provide bus response information from device response information using the device select signal; and

a de-multiplexer coupled to the second multiplexer and the first and second master buses to transfer the bus response information to one of the first and second processors using the arbitration select signal.

25. The system of claim 24 wherein the device response information includes at least one of device ready status and read data.

26. The system of claim 25 further comprising:

a common memory coupled to the plurality of slave buses via a common memory interface to provide access to one of the first and second processors.

27. The system of claim 25 wherein one of the first and second processors is a direct memory access (DMA) controller.

28. The system of claim 25 wherein one of the first and second processors is a microprocessor.

29. The system of claim 25 wherein the first slave device is one of a memory device and a peripheral device.

30. The system of claim 5 wherein the plurality of slave buses includes at least one of a homogenous set and a heterogeneous set.